PURWANCHAL UNIVERSITY
VII SEMESTER FINAL EXAMINATION-2004

LEVEL : B. E. (Electronics & communication)
SUBJECT: BEG474CO, Computer Architecture.
Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
All questions carry equal marks. The marks allotted for each sub-question is specified along its side.
Attempt ALL questions.

Q. [1] **[a]**Explain the structure and functions of different component of a computer system. [8]
[b] What is PCI bus? Why is it used? [2]

Q. [2] **[a]**What are internal memories? Explain how binary values are stored and read from a SRAM cell with neat diagram. [2+4]
[b]What are I/O modules? Why do we need it? Give An example if I/O module. [4].

Q. [3] **[a]**How do we represent a floating-point number? Represent the number $(+46.5)_{10}$ as a floating-point Binary number with 24bits. The normalized fraction Mantissa has 16 bits and exponents has 8-bits. [2+4]
[b]What are different types of operation found on a Computer system? Explain.
[4]

Q. [4] **[a]**What are registers? Explain the organization of Register in computer system. [4]
[b]What do you mean by instruction pipelining? Explain with suitable examples. [4]
[c]Give the format of the flag register for Pentium II Processor. [2]

Q. [5] **[a]**What are RISC? What are the characteristics for RISC? [5]
[b]How are register optimized by the compiler? [5]

Q. [6] **[a]**What are micro-operations? Give the micro-operation for the following Add instruction: [5]
Add R1, X

Q. [7] **[a]**What do you mean by cache coherence problem? Explain MESI protocol. [2+6]
[b]What are different types of parallel processing system? [2]

Q. [8] Write short notes on: [2×5=10]
[a] Vector computing
[b] Application of microprogramming.

PURWANCHAL UNIVERSITY
VII SEMESTER BACK-PAPER EXAMINATION-2004

LEVEL : B. E. (Electronics & communication)
SUBJECT: BEG474CO, Computer Architecture.
Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
All questions carry equal marks.
Attempt Any EIGHT questions.

Q.[1] Differenciate between Computer organization and computer architecture. Give a brief history about the evolution of computer.

Q.[2] Give the overview of Von Nenumann architecture. Explain how instruction processing is done by the computer. Using appropriate diagram.

Q.[3] Differentiate between external and internal memory. How floating type data are represented? Explain with example.

Q.[4] what do you mean by pipelining? Pipeline the following set of instructions:

Instruction1: MOV A,B
Instruction2: MOV C,D
Instruction3: ADD C

Explain branch prediction method of dealing branches in pipelining.

Q.[5] Differentiate between RISC an CISC. Explain complier based register optimization technique of RISC.

Q.[6] Define micro-operations. Explain hardwired implementation method of control unit.

Q.[7] What are the two basic tasks performed by micro-programmed control unit? Explain micro-instructions sequencing.

Q.[8] Classify the parallel processors. What do you mean by cache-coherence? If it is the problem, suggest a method to solve it.

Q.[9] How we increase the performance of a computer by adopting vector computation? Explain with an example. Make the differences between instruction pipelining and vector processing.

PURWANCHAL UNIVERSITY
VII SEMESTER FINAL EXAMINATION-2005
LEVEL : B. E. (Electronics & communication)
SUBJECT: BEG474CO, Computer Architecture.
Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
All questions carry equal marks. The marks allotted for each sub-questions is specified along its side.
Attempt Any EIGHT questions.

Q.[1] Explain Structure and Functions. Write short note on power PC evolution. [10]

Q.[2] Draw the Schematic Block diagram of a Computer. [10]

Q.[3] How does Operating System Support as a interpreter for certain Architectural features? Explain [10]

Q.[4] **[a]** How are number expressed in Floating Point Notation? Why are floating point number Normalized? [5]
[b] Show how the following two floating point numbers are to be added to get a normalized result. [5]
$(-0.12467\times10^{4})+(+0.71340\times10^{-1})$

Q.[5] A two word instruction is stored in memory at an address designated by symbol W. The address field of the instruction (stored at W+1) is designated by th symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by z. An index register contains the value X. State how Z is calculated from the other address if the addressing mode of the instruction is:
a) Direct (b) indirect (c) relative (d) indexed.

Q.[6] Explain four possible hardware schemes that can be used in an instruction pipeline in order to minimize performance degradation caused by instruction branching.

Q.[7] Explain the difference between hardwired control and micro programmed control. It is possible to have a harwird control associated with a control memory? [10]

Q.[8] What is Cache Coherence? Why is it important in Sha…memory multiprocessor systems? How can this problem be solved? [10]

Q.[9] Write Short notes on: [2×5=10]
[a] Machine Instruction Characteristics.
[b] Vector Computation.
[c] PCI

PURWANCHAL UNIVERSITY
VII SEMESTER BACK-PAPER EXAMINATION-2005
LEVEL : B. E. (Electronics & communication)
SUBJECT: BEG474CO, Computer Architecture.

Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
All questions carry equal marks. .
Attempt Any FIVE questions. [5×16]

Q.[1] Discuss about instruction pipelining.

Q.[2] **[a]** What is performance penality? How can you overcome it?
[b] Discuss about instruction cycle with suitable diagram.

Q.[3] Describe the difference between RISC and CISC architecture. Describe the architecture of RISC system.

Q.[4] List and briefly define the key services provided by an operating system. Discuss one of the efficient techniques in memory management system.

Q.[5] **[a]** List and briefly explain five important instruction set design issues.
[b] Discuss about interconnection structure.

Q.[6] **[a]** Describe penitum processor registers.
[b] Discuss the advantage of cache memory.

Q.[7] Write short notes on (any TWO):
[a] Microperation.
[b] Power PC on Penitum interrupts processing (handling).
[c] Addressing Node.

PURWANCHAL UNIVERSITY
VII SEMESTER FINAL EXAMINATION-2006

LEVEL : B. E. (Electronics & communication)
SUBJECT: BEG474CO, Computer Architecture.

Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
All questions carry equal marks. The marks allotted for each sub-question is specified along its side.
Attempt ALL questions.

Q.[1] **[a]**Give a brief history about the evolution of computer? [6]
[b]Explain structure and function of a computer system. [4]

Q.[2] **[a]**What are internal memories. Explain DRAM and SRAM with neat diagram. [6]
[b]What are I/O modules? Why do we need it? Give an example of I/O modules. [4]

Q.[3] **[a]**Explain DRAM and their function. [3]
[b]What are seek time, rotational delay and transfer time? [3]
[c] What is scheduling? Explain their types. [4]

Q.[4] **[a]**Explain paging. How logical addresses are translated to physical address?
[b]Explain different addressing modes in computer system. [3]
[c]What do you mean by instruction pipelining ? Explain the organization of register in computer system. [3]

Q.[5] **[a]**Difference between RISC and CISO. Explain complier based register optimization techniques of RISC. [8]
[b]What is windows register? Explain. [2]

Q.[6] **[a]**What are micro-oprations? Give the micro-operation for the following add instruction:
Add R1, X [5]
[b] Explain the hardwired implementation of control unit. [5]

Q.[7] **[a]**What do you mean by cache coherence problem? Explain MESI protocol. [2+6]
[b] What are different types of parallel processing system? [2]

Q.[8] **Write short notes on:** [2×5=10]
[a] Application of microprogramming.
[b] Vector computing

PURWANCHAL UNIVERSITY
VII SEMESTER FINAL EXAMINATION-2007

LEVEL : B. E. (Electronics & communication)
SUBJECT: BEG474CO, Computer Architecture.
Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
All questions carry equal marks. The marks allotted for each sub-question is specified along its side.
Attempt any EIGHT questions.

Q.[1] **[a]**Discuss the impact of advances in semiconductor technology on evolution of computer system. [5]
[b]What are the Bus design features? Compare different Bus configuration. [5]

Q.[2] Define precision and range of representation. Explain biased exponent. Represent +-21 into single precison format. [10]

Q.[3] **[a]**Explain the various functions of operating system. [5]
[b]Explain PCI. Differentiate external memory form internal memory. [5]

Q.[4] **[a]**Multiply 5*-4 using Booth's algorithm. [6]
[b]What are different types of operation found on computer system explain. [4]

Q.[5] **[a]**Explain processor organization with detail diagram containing arithmetic logical unit and control unit with associative register. [6]
[b]Explain instruction pipelining with example. [4]

Q.[6] **[a]**Explain graph coloring methods to optimize the use of register. [5]
[b] Explain RISC Vs CISC controversy. [5]

Q.[7] **[a]**Define micro-operation. Write micro operaton for fetch and interrupt cycle. [5]
[b]Explain micro program sequencing. What are the advantages of micro programmed control over hardwired control? [5]

Q.[8] **[a]** What is multiple processing. Explain cache coherence problem. [5]
[b]What are the different types of parallel processing ? [5]

Q.[9] Write short note on: [4×2.5=10]
[a] Power PC
[b] Paging in memory management.
[c] Vector computation.
[d] MESI protocol.

PURWANCHAL UNIVERSITY
VII SEMESTER FINAL EXAMINATION-2008

LEVEL : B. E. (Electronics & communication)
SUBJECT: BEG474CO, Computer Architecture.

Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
All questions carry equal marks. The marks allotted for each sub-question is specified along its side.
Answer FIVE questions.

Q.[1] **[a]**Define function and structure. Describe four main structural components of a commuter briefly. [5]
[b]Draw the bus configurations of traditional bus architecture and high performance architecture and distinguish between these configurations. [6]
[c]Distinguish between programmed I/O and interrupt driven I/O showing the flowchart of their operation. [5]

Q.[2] **[a]** Represent the following decimal numbers in both signed magnitude and two's complement form using 16 bits: (i) +256, (ii) -30 [4]
[b] What are the elements of machine instruction? Describe briefly the types of operands. [6]
[c] Describe briefly the sub cycles of an instruction cycle with the help of instruction cycle state diagram. [6]

Q.[3] **[a]**Describe briefly the basic addressing modes. [5]
[b]List and briefly explain the services provided by an opeariong system. [4]
[c]Distinguish between horizontal and vertical micro-instruction. Describe the basic sequencing techniques of a micro-instruction. [7]

Q.[4] **[a]**Explain the pipelining in strategy of instructions with the help of timing diagram. Also discuss how it deals with the conditional branch instruction. [8]
[b]What are the typical characteristics of reduced instruction set architecute? Also, discuss the use of large register file on RISC machine and its difference from cache Memory. [8]

Q.[5] **[a]**Distinguish between hardwired control unit and micro-programmed control unit. [4]
[b]Give the block diagram of a control unit. What are the basic tasks performed by a control unit? [4]
[c] Describe the types of control and status registers of a computer system briefly. [4]
[d] Describe the function of micro programmed control unit wit its clear schematic. [4]

Q.[6] **[a]**What are different types of parallel processor system? List the advantages of symmetric multiprocessor over a uniprocessror.[5]
[b] How cache coherence problem arises in a multiprocessor system? Give the meaning of each of four states in MESI protocol? [6]
[c] Discuss the graph coloring approach used in the RISC compliers. [5]

PURWANCHAL UNIVERSITY
VII SEMESTER BACK-PAPER EXAMINATION-2008

LEVEL : B. E. (Electronics & communication)
SUBJECT: BEG474CO, Computer Architecture.

Full Marks: 80
TIME: 03:00 hrs **Pass marks:** 32

Candidates are required to give their answers in their own words as far as practicable.
All questions carry equal marks. The marks allotted for each sub-question is specified along its side.
Answer EIGHT questions.

Q.[1] **[a]**What are basic characteristic based on which next generation of computer systems are expected to be built? [5]
[b]Differentiate between computer system architecture and computer organization. [5]

Q.[2] Define precision and range of representiaton. Explain biased exponent. Represent +-1/16 into signle precison format. [10]

Q.[3] **[a]**Explain the bus interconnection structure. What are the different types of bus in a computer system? [5]
[b]Explain the structure and function of general computer system. [5]

Q.[4] **[a]**Draw a flow chart of Booth's algorithm for multiplication. [6]
[b]What do you mean by Addressing mode? Explain any four addressing modes used in instructions. [4]

Q.[5] **[a]**Explain processor organization with detail diagram containing arithmetic unit, logical unit and control unit with associative register. [6]
[b]Explain instruction pipelining with example. [4]
]

Q.[6] **[a]**Explain Compiler-based register opmization with example. [5]
[b] What are the characteristics of Reduced Instrucion ser architecture? [5]

Q.[7] **[a]**Define Instruction cycle. Write micro operation for fetch and insterrupt cycle. [5]
[b] Explain micro program sequencing. What are the applications of micro-progarmmed control? [5]

Q.[8] **[a]**What is multiprocessing? Explain cache coherence problem in multiprocessor organization. [5]
[b]What are the different types of parallel processing? [5]

Q.[9] **Write short note on**: [4×2.5=10]
[a] Pentium Processor.
[b] CPU Scheduling.
[c] Hardwired Control
[d] Seek time, Rotational delay, transfer time.